UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/520,677	03/07/2000	Garry Z. Gu	56115534-120430	9129

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EXAMINER
VOLPER, THOMAS E

ART UNIT	PAPER NUMBER
2697	

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

    A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____ .

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-18* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-5,10-12 and 15-17* is/are rejected.

7) ☒ Claim(s) *6-9,13,14 and 18* is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *07 March 2000* is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)   4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5) ☐ Notice of Informal Patent Application (PTO-152)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .   6) ☐ Other: .

DETAILED ACTION

Drawings

1.   The drawings are objected to because they contain hand written labeling. A proposed

drawing correction or corrected drawings are required in reply to the Office action to avoid

abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claims 1-5, 10-12 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Caldara et al. (US 5,978,359) in view of Larsson et al. (US 6,172,963).

- Regarding claim 1, 10 and 11, Caldara discloses a switching architecture that includes a

first set of port processors, called To Switch Port Processors (TSPP) (14) and a second set of port

processors, called From Switch Port Processors (FSPP) (16). These sets of TSPP's and FSPP's

can be construed as representing first and second stages in the switch, respectively. Caldara also

discloses a feedback message (30) that provides an indication of buffer status at the output port.

This message is sent in response to a request message (36), which is interpreted to represent the

data packet of the present invention (col. 5, line 53-61). To provide efficient flow control, the

feedback message from the output port to the input port includes several sub-type messages,

including an ACCEPT/ REJECT bit (col. 5, line 64 – col. 6, line 14). This bit is considered to

provide the function of the token bit of the applicant's invention. Caldara discloses it is

determined if the output buffers become filled to a threshold level when sending the feedback

message in order to prevent cell loss (col. 4, lines 37-53). It is obvious that some component,

such as a statistic block as in the present application, must count the number of cells in the output

buffers and compare them to a threshold level in order to obtain this result. Caldara does not

expressly disclose granting credit and an integrator block located in the port processor of the first

stage. Larsson discloses a credit-based flow control system for a switch with input and output

buffers. The system takes into account the degree of fullness of the output buffers when

determining how many cells (credits) can be sent from each input port. This process is called

"giving credit" (col. 3, lines 21-30). Each input port is divided into as many FIFO memories

(41-43) as there are output ports. With intelligence in the switch, it can be determined which

output ports are able to receive cells, how many cells, and from which FIFO memories (col. 4,

lines 45-55). In the preferred embodiment, Larsson discloses a control unit (20) located in the

switch core (8) for performing the intelligence. However, the intelligence may also be located

outside the switch core and incorporated into the input buffers. In this case, the input ports

would read the degree of fullness of the output buffers and calculate how many cells can be sent

(col. 5, lines 12-23). This description meets the limitation of an integrator block as in the present

application. The limitation of neighboring integrator blocks is met by the fact that each input

port has multiple FIFO memories, one for each output port. In the case that the intelligence was

located in the input port of Larsson, multiple intelligences, i.e. multiple integrator blocks, would

be necessary to perform the intelligence of each of these FIFO memories. At the time the

invention was made, it would have been obvious to a person of ordinary skill in the art to use the architecture and feedback message of Caldara in combination with the credit based flow control system of Larsson to provide a switch that selectively sends data from a first stage of input ports to a second stage of output ports in accordance with the fullness or availability of each output buffer. The feedback message of Caldara would notify the intelligent input ports of Larsson as to the availability of the output ports in order to calculate the credit given to each input port. One of ordinary skill in the art would have been motivated to do this to provide efficient flow control and avoid cell loss in the switch.

- Regarding claims 2 and 3, Larsson discloses multiple FIFO memories (41-43) within one input port that are stacked on top of each other. The aforementioned teaching regarding claims 1 and 10 provides a description for the incorporation of intelligence into the input port for each of these FIFO memories. This description provides for an equivalent to neighboring integrator blocks.

- Regarding claims 4, 5, 12, 16 and 17, Larsson discloses that the number of cells (credits) that can be sent are calculated for a time interval and depend on the number of cells already in the output buffers (col. 3, lines 45-58). It is possible, depending on the fullness of the output buffers from interval to interval, that the number of credits will change. This effectively achieves the process of incrementing and decrementing credits between time intervals.

- Regarding claim 15, Fig. 1 shows two TSPP's coupled to the switch fabric (10) directly adjacent to one another.

Allowable Subject Matter

4.   Claims 6-9, 13, 14 and 18 are objected to as being dependent upon a rejected base claim,

but would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims.

5.   The following is a statement of reasons for the indication of allowable subject matter:

- Regarding claims 6, 13 and 14, the prior art fails to disclose sending a data packet from

an input port to an output port having the maximum number of grant credits within the first

stage.

- Regarding claim 7, the prior art fails to disclose third stage port processors and that the

statistics block accumulates real-time statistics of data packet departures to the third stage port

processors.

- Regarding claim 8, the prior art fails to disclose a relay from third stage port processors

to first stage port processors, and sending the token bit from the third stage to the first stage.

- Regarding claim 9, the prior art fails to disclose third stage switch elements on a single

chip with first stage elements.

- Regarding claim 18, the prior art fails to disclose that the statistics block departs the

data packet that was sent that triggers a token bit to be sent.

Conclusion

6.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

- McClure et al. (US 5,790,770) Method and Apparatus for Reducing Information Loss in

a Communication Network

    - Chiussi et al. (US 5,689,500) Multistage Network Having Multicast Routing Congestion

Feedback

    - Manning et al. (US 5,917,805) Network Switch Utilizing Centralized and Partitioned

Memory for Connection Topology Information Storage

7.   Any inquiry concerning this communication, or earlier communications from the

examiner should be directed to Thomas Volper whose telephone number is 703-305-8405 and

fax number is 703-746-9467. The examiner can normally be reached between 9:00am and

6:30pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Ricky Ngo, can be reached at 703-305-4798. Any inquiry of a general nature or

relating to the status of this application or proceeding should be directed to the receptionist

whose telephone number is 703-305-4750.

tev

May 16, 2003

RICKY NGO
PRIMARY EXAMINER